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PATENT

IN THE UNITED STATE PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Leo Carl Christensen
For	:	TECHNIQUE FOR CREATING A MACHINE TO ROUTE NON-PACKETIZED DIGITAL SIGNALS USING DISTRIBUTED RAM
Serial No.:	:	09/739,506
Filed	:	December 18, 2000
Art Unit	:	2668
Examiner	:	S. Blount
Att. Docket	:	US 000344
Confirmation No.	:	3124

APPEAL BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

This Appeal Brief is submitted in response to the Final Office Action dated January 10, 2006, in support of the herewith enclosed Notice of Appeal.

I. REAL PARTY IN INTEREST

The party in interest is the applicant, PHILIPS ELECTRONICS NORTH AMERICA CORPORATION.

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II. RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

III. STATUS OF CLAIMS

This is an appeal from the Final Office Action dated January 10, 2006 rejecting claims 1 and 3-11. Claim 2 stands cancelled. No other claims are pending in the application. The claims being appealed are claims 1 and 3-11.

IV. STATUS OF AMENDMENTS

All Amendments filed in this application have been entered. A correct copy of appealed claims 1 and 3-11, including all entered amendments thereto, appears in the attached Claims Appendix.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a digital signal router and a method of routing digital signals from N inputs to M outputs using distributed RAM.

Claim 1 (independent – signal router)

The signal router, as claimed in independent claim 1, comprises: a conditioning circuit configured to write K identical images (Fig. 2; page 5, lines 19-21; and page 8, line 15) of a first parallel set of data from N inputs to K random access memories during a first time interval; and K respective bit selectors (Figs. 1-2 and page 6, line 20-page 7, line 3) each configured to read

respective portions of a respective one of said K identical images. Said K respective bit selectors are coupled to construct M output data streams (Figs. 1-2 and page 6, line 23-page 7, line 3) during a second time interval. **Each of the random access memories comprises exactly two parts** (Fig. 2 and page 8, lines 13-21) configured so that during the second time interval a read occurs from a first one of the parts, while a write occurs to a second one of the parts (page 8, line 23 to page 9, line 5).

Claim 4 (independent – signal router)

The signal router, as claimed in independent claim 4, comprises a controller programmed to store identical images (Fig. 2; page 5, lines 19-21; and page 8, line 15) of parallel data from N inputs in K memories. Said controller is further programmed to read respective bits of said data from each of said K memories to produce M respective output data streams (Figs. 1-2 and page 6, line 23-page 7, line 3), whereby N inputs are mapped to M outputs. **Each of the K memories comprises exactly two parts** (Fig. 2 and page 8, lines 13-21) configured so that during the second time interval a read occurs from a first one of the parts, while a write occurs to a second one of the parts(page 8, line 23 to page 9, line 5).

Claim 7 (independent – method of routing data)

As claimed in claim 7, the method of routing data from N inputs to M outputs, comprises the steps of: applying parallel data from said N inputs to a data buss by means of at least one of time and space multiplexing; imaging said parallel data on K random access memories from said buss; and reading respective sets of bits from said random access memories to form respective ones of said signals ultimately demultiplexed to form said M outputs (Figs. 1-2 and page 6, line 23-page 7, line 3), wherein **each of the random access memories comprises exactly two parts** (Fig. 2 and page 8,

lines 13-21) configured so that during the second time interval a read occurs from a first one of the parts, while a write occurs to a second one of the parts (page 8, line 23 to page 9, line 5).

Claim 11 (independent – signal router)

The signal router, as claimed in independent claim 11, comprises: N inputs for receiving synchronous streams of serial broadcast data; a conditioning circuit configured to write K identical images (Fig. 2; page 5, lines 19-21; and page 8, line 15) of a first set of parallel data from the N inputs to K memories during a first time interval; and K respective bit selectors (Figs. 1-2 and page 6, line 20-page 7, line 3), each configured to read respective portions of a respective one of said K identical images. Each of said K respective bit selectors is coupled to construct M output data streams during a second time interval (page 8, line 23 to page 9, line 5).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A.. Claims 1 and 3-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 3,761,894 to Pile et al. ("Pile") in view of US Patent No. 6,208,641 to Ruuskanen et al. ("Ruuskanen").

B. Claim 11 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the alleged "Applicant's Admitted Prior Art" ("AAPA") in view of Pile and Ruuskanen.

VII. ARGUMENT

In the Final Office Action dated 01/10/2006, the Examiner reiterated the rejection of claims 1 and 3-10 under 35 U.S.C. § 103(a), using Pile as a primary reference and relying upon Ruuskanen as a secondary reference. The Examiner also reiterated his previous rejection of claim 11 under 35 U.S.C. § 103(a), using the alleged AAPA as a primary reference and relying upon the combined Pile and Ruuskanen as a secondary reference.

The *prima facie* test for obviousness is set forth by M.P.E.P. § 2143:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Appellant will show that the prior art references cited by the Examiner do not teach or suggest all the claim limitations, as recited in each of the independent claims 1, 4, 7 and 11, and consequently in any of their respective dependent claims.

A. Rejection of Claims 1 and 3-10 under 35 U.S.C. §103(a)

Claims 1 and 3-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 3,761,894 to Pile et al. ("Pile") in view of US Patent No. 6,208,641 to Ruuskanen et al. ("Ruuskanen").

Claims 1, 3 and 8

Appellant respectfully submits that Pile does not teach "each of the random access memories **comprises exactly two parts**" as set forth in independent claim 1. What Pile shows is "each outgoing path is provided with **two memories sets**" (Col. 2:32-33), and "data from the data bus is written into **one set of memories** and stored data is read out from the **other set** to the associated outgoing path." (Col. 2:34-36) In other words, the present invention only requires one set of memories, thereby reducing complexity and manufacturing cost, whereas Pile requires two separate sets of memories. Appellant also submits that Ruuskanen does not cure this deficiency because the switching memory used by Ruuskanen to store the data does not comprise exactly two parts as recited in the claims of the present application. The only memory comprising two parts in Ruuskanen is the control memory CM, which is not used to store the actual signal data but only addresses : "the first part CM1 stores the read addresses of the switching memory SM and the bits of the second part CM2 control a selector SEL." (Col. 4:6-8). It is therefore submitted that the cited art references do not, each in itself or in combination, teach or suggest all the claim limitations.

Additionally, Appellant notes that the Examiner admitted in the Final Office Action dated 01/10/2006 that Pile does not teach "a signal transducer configured to **write K identical images**" "to

K random access memories" as set forth in claim 1, and relied upon Ruuskanen for that feature. However, Ruuskanen also teaches at Col. 4:66 to Col. 5:4: "If the read rate of the switching memory SM can be increased to be four-fold in relation to the write rate, **the switching memory need not be replicated**, but all four control memory-register-selector combinations may **use a switching memory in common**." This, Appellant submits, teaches away from the signal router of the present invention as set forth in claim 1, which recites **"K random access memories"**.

Furthermore, Appellant submits that Ruuskanen teaches away from Pile by suggesting that "the **read rate** of the switching memory SM **can be increased to be four-fold in relation to the write rate**" because Pile clearly states at Col. 2:9-13: "It is therefore an object of this invention to provide a memory system having a **high access rate during** one cycle, such as the **write-in cycle**, and a relatively **low access rate during** the other cycle, such as the **read-out cycle**." and also at Col. 2:29-31: "Since storage areas are simultaneously read out, all the areas can be accessed at the **lower out-going path signaling rate**." In other words, Ruuskanen suggests that it would be advantageous to have a read-out rate of the switching memory higher than its write-in rate, whereas one object of Pile's invention is precisely the opposite.

Accordingly, Claim 1 is patentable over Pile in view of Ruuskanen because all claims limitations are neither taught nor suggested. Furthermore, Appellant submits that, not only is there no teaching or suggestion in the references to combine reference teachings, but also that there could be no motivation to combine the cited art references because these references actually teach away from each other. Reconsideration and withdrawal of the rejection of Claim 1 is therefore respectfully requested.

Claim 3 depends from Claim 1 and further claims that the conditioning circuit includes a buss to which the first set of data is applied, and addressing controllers configured to write data from the buss to the random access memories, whereby K identical images are written. Accordingly, Claim 3 is allowable for at least the reason that Claim 1 is patentable as well as for the separately patentable elements contained in Claim 3.

Claim 8 depends from Claim 1 and further claims that the parts of the random access memories are configured so that upon completion of the second interval, the first and second parts change roles, so that subsequently the first part is used for the write and the second part is used for the read. Accordingly, Claim 8 is allowable for at least the reason that Claim 1 is patentable as well as for the separately patentable elements contained in Claim 8.

Claims 4-6 and 9

Appellant respectfully submits that Pile does not teach "each of the random access memories **comprises exactly two parts**" as set forth in independent claim 4. What Pile shows is "each outgoing path is provided with **two memories sets**" (Col. 2:32-33), and "data from the data bus is written into **one set of memories** and stored data is read out from the **other set** to the associated outgoing path." (Col. 2:34-36) In other words, the present invention only requires one set of memories, thereby reducing complexity and manufacturing cost, whereas Pile requires two separate sets of memories. Appellant also submits that Ruuskanen does not cure this deficiency because the switching memory used by Ruuskanen to store the data does not comprise exactly two parts as recited in the claims of the present application. The only memory comprising two parts in

Ruuskanen is the control memory CM, which is not used to store the actual signal data but only addresses : "the first part CM1 stores the read addresses of the switching memory SM and the bits of the second part CM2 control a selector SEL." (Col. 4:6-8). It is therefore submitted that the cited art references do not, each in itself or in combination, teach or suggest all the claim limitations.

Additionally, Appellant notes that the Examiner admitted in the Final Office Action dated 01/10/2006 that Pile does not teach "a signal transducer configured to **write K identical images**" "to K random access memories" as set forth in claim 4, and relied upon Ruuskanen for that feature. However, Ruuskanen also teaches at Col. 4:66 to Col. 5:4: "If the read rate of the switching memory SM can be increased to be four-fold in relation to the write rate, **the switching memory need not be replicated**, but all four control memory-register-selector combinations may **use a switching memory in common**." This, Appellant submits, teaches away from the signal router of the present invention as set forth in claim 1, which recites "**K random access memories**".

Furthermore, Appellant submits that Ruuskanen teaches away from Pile by suggesting that "the **read rate** of the switching memory SM **can be increased to be four-fold in relation to the write rate**" because Pile clearly states at Col. 2:9-13: "It is therefore an object of this invention to provide a memory system having a **high access rate during** one cycle, such as the **write-in cycle**, and a relatively **low access rate during** the other cycle, such as the **read-out cycle**." and also at Col. 2:29-31: "Since storage areas are simultaneously read out, all the areas can be accessed at the **lower out-going path signaling rate**." In other words, Ruuskanen suggests that it would be advantageous to have a read-out rate of the switching memory higher than its write-in rate, whereas one object of Pile's invention is precisely the opposite.

Accordingly, claim 4 is patentable over Pile in view of Ruuskanen because all claims limitations are neither taught nor suggested. Furthermore, Appellant submits that, not only is there no teaching or suggestion in the references to combine reference teachings, but also that there could be no motivation to combine the cited art references because these references actually teach away from each other. Reconsideration and withdrawal of the rejection of claim 4 is therefore respectfully requested.

Claim 5 depends from Claim 4 and further claims a data buss connected to receive said N inputs and distribute them to said K memories, wherein pre-sorting of the input data is not necessary. Accordingly, Claim 5 is allowable for at least the reason that Claim 4 is patentable as well as for the separately patentable elements contained in Claim 5.

Claim 6 depends from Claim 5 and further claims that the bit rate of each of said M outputs streams is less than the bit rate of the buss. Accordingly, Claim 6 is allowable for at least the reason that Claim 5 is patentable as well as for the separately patentable elements contained in Claim 6.

Claim 9 depends from Claim 4 and further claims that the parts of the random access memories are configured so that upon completion of the second interval, the first and second parts change roles, so that subsequently the first part is used for the write and the second part is used for the read. Accordingly, Claim 9 is allowable for at least the reason that Claim 4 is patentable as well as for the separately patentable elements contained in Claim 9.

Claims 7 and 10

Appellant respectfully submits that Pile does not teach "each of the random access memories **comprises exactly two parts**" as set forth in independent claim 7. What Pile shows is "each outgoing path is provided with **two memories sets**" (Col. 2:32-33), and "data from the data bus is written into **one set of memories** and stored data is read out from the **other set** to the associated outgoing path." (Col. 2:34-36) In other words, the present invention only requires one set of memories, thereby reducing complexity and manufacturing cost, whereas Pile requires two separate sets of memories. Appellant also submits that Ruuskanen does not cure this deficiency because the switching memory used by Ruuskanen to store the data does not comprise exactly two parts as recited in the claims of the present application. The only memory comprising two parts in Ruuskanen is the control memory CM, which is not used to store the actual signal data but only addresses : "the first part CM1 stores the read addresses of the switching memory SM and the bits of the second part CM2 control a selector SEL." (Col. 4:6-8). It is therefore submitted that the cited art references do not, each in itself or in combination, teach or suggest all the claim limitations.

Additionally, Appellant notes that the Examiner admitted in the Final Office Action dated 01/10/2006 that Pile does not teach "a signal transducer configured to **write K identical images**" "to K random access memories" as set forth in claim 1, and relied upon Ruuskanen for that feature. However, Ruuskanen also teaches at Col. 4:66 to Col. 5:4: "If the read rate of the switching memory SM can be increased to be four-fold in relation to the write rate, **the switching memory need not be replicated**, but all four control memory-register-selector combinations may **use a switching memory in common.**" This, Appellant submits, teaches away from the signal router of the present invention as set forth in claim 1, which recites "**K random access memories**".

Furthermore, Appellant submits that Ruuskanen teaches away from Pile by suggesting that "the **read rate** of the switching memory SM **can be increased to be four-fold in relation to the write rate**" because Pile clearly states at Col. 2:9-13: "It is therefore an object of this invention to provide a memory system having a **high access rate during** one cycle, such as the **write-in cycle**, and a relatively **low access rate during** the other cycle, such as the **read-out cycle.**" and also at Col. 2:29-31: "Since storage areas are simultaneously read out, all the areas can be accessed at the **lower out-going path signaling rate.**" In other words, Ruuskanen suggests that it would be advantageous to have a read-out rate of the switching memory higher than its write-in rate, whereas one object of Pile's invention is precisely the opposite.

Accordingly, claim 7 is patentable over Pile in view of Ruuskanen because all claims limitations are neither taught nor suggested. Furthermore, Appellant submits that, not only is there no teaching or suggestion in the references to combine reference teachings, but also that there could be no motivation to combine the cited art references because these references actually teach away from each other. Reconsideration and withdrawal of the rejection of claim 7 is therefore respectfully requested.

Claim 10 depends from Claim 7 and further claims that the parts of the random access memories are configured so that upon completion of the second interval, the first and second parts change roles, so that subsequently the first part is used for the write and the second part is used for the read. Accordingly, Claim 10 is allowable for at least the reason that Claim 7 is patentable as well as for the separately patentable elements contained in Claim 10.

B. Rejection of Claim 11 under 35 U.S.C. §103(a)

Appellant incorporates herein by reference the arguments presented above against the rejection of Claims 1 and 3-10 under 35 U.S.C. § 103(a) over Pile in view of Ruuskanen. In the Final Office Action dated January 10, 2006, the Examiner cited parts of Appellant's present application and labeled them "Applicant's Admitted Prior Art." However, Appellant submits that the statement "There is a perennial need for switches that handle digital data synchronously, and that must remain time aligned, and that do not grow in complexity too fast as the endpoint capacity of the switch increases" cannot be construed as the alleged AAPA, as the Examiner does. This statement sets forth the need that the present invention is meant to fulfill, not the state of the prior art. The Appellant strongly disagrees with the Examiner's characterization of this portion of the specification as alleged AAPA.

The Examiner admitted in the Final Office Action that the alleged AAPA does not teach "the solution to this problem in the broadcasting systems to comprise writing identical images to memory during a first time interval, and reading them in a second time interval, including the use of bit selectors." The Examiner relies upon the combined Pile/Ruuskanen for "this type of a system." However, Appellant submits that these references cannot be combined for at least the reasons set forth in the arguments presented above against the rejection of Claims 1 and 3-10 under 35 U.S.C. § 103(a) over Pile in view of Ruuskanen, and therefore Claim 11 cannot be obvious over the alleged AAPA in view of Pile/Ruuskanen.

Accordingly, Appellant submits that Claim 11 is patentable over the cited art references because all the claim limitations are neither taught nor suggested, and furthermore because there is no suggestion or motivation to combine the cited art references.

VIII. CONCLUSION

Appellant submits that all the claims on appeal are patentable because they are neither anticipated nor suggested by the cited art references. Accordingly, reversal of all the rejections and allowance of all the claims submitted on appeal is respectfully solicited.

Respectfully submitted,
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April 10, 2006
Date

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CLAIMS APPENDIX

1. A signal router, comprising:

a conditioning circuit configured to write K identical images of a first parallel set of data from N inputs to K random access memories during a first time interval;

K respective bit selectors each configured to read respective portions of a respective one of said K identical images;

said K respective bit selectors being coupled to construct M output data streams during a second time interval

wherein each of the random access memories comprises exactly two parts configured so that during the second time interval a read occurs from a first one of the parts, while a write occurs to a second one of the parts.

(Claim 2: Canceled)

3. A signal router, as in claim 1, wherein said conditioning circuit includes a buss to which said first set of data is applied and addressing controllers configured to write data from said buss to said random access memories, whereby said K identical images are written.

4. A signal router, comprising:

a controller programmed to store identical images of parallel data from N inputs in K memories;

said controller being further programmed to read respective bits of said data from each of said K memories to produce M respective output data streams, whereby N inputs are mapped to M outputs,

wherein each of the K memories comprises exactly two parts configured so that during the second time interval a read occurs from a first one of the parts, while a write occurs to a second one of the parts.

5. A router as in claim 4, further comprising a data buss connected to receive said N inputs and distribute them to said K memories, wherein pre-sorting of the input data is not necessary.

6. A router as in claim 5, wherein a bit rate of each of said M output streams is less than a bit rate of said buss.

7. A method of routing data from N inputs to M outputs, comprising the steps of:

applying parallel data from said N inputs to a data buss by means of at least one of time and space multiplexing;

imaging said parallel data on K random access memories from said buss;

reading respective sets of bits from said random access memories to form respective ones of said signals ultimately demultiplexed to form said M outputs,

wherein each of the random access memories comprises exactly two parts configured so that during the second time interval a read occurs from a first one of the parts, while a write occurs to a second one of the parts.

8. The router of claim 1, wherein the parts are configured so that upon completion of the second interval, the first and second parts change roles, so that subsequently the first part is used for the write and the second part is used for the read.

9. The router of claim 4, wherein the parts are configured so that upon completion of the second interval, the first and second parts change roles, so that subsequently the first part is used for the write and the second part is used for the read.

10. The method of claim 7, wherein the parts are configured so that upon completion of the second interval, the first and second parts change roles, so that subsequently the first part is used for the write and the second part is used for the read.

11. A signal router, comprising:

N inputs for receiving synchronous streams of serial broadcast data;

a conditioning circuit configured to write K identical images of a first set of parallel data from the N inputs to K memories during a first time interval;

K respective bit selectors each configured to read respective portions of a respective one of said K identical images; and

each of said K respective bit selectors being coupled to construct M output data streams during a second time interval.

Application No: 09/739,506
Attorney's Docket No: US 000344

EVIDENCE APPENDIX

Listing and copies of evidence relied upon by the Examiner as to grounds of rejection to be reviewed on Appeal:

1. US Patent No. 3,761,894 to Pile et al. was relied upon by the Examiner as a primary reference and as a secondary reference for § 103(a) rejections in the Final Office Action dated 01/10/2006.

2. US Patent No. 6,208,641 to Ruuskanen et al. was relied upon by the Examiner as a secondary reference for § 103(a) rejections in the Final Office Action dated 01/10/2006.

3. The specification in Appellant's present application was relied upon by the Examiner as a primary reference for a §103(a) rejection in the Final Office Action dated 01/10/2006.

Application No: 09/739,506
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RELATED PROCEEDINGS APPENDIX

None.